REMARKS

Claims 1, 21, 40-41, and 46 have been amended. Claims 43-45 have been cancelled. No new claims have been added. Thus, claims 1-42 and 46-61 are pending.

Claims 1-61 stand rejected as being anticipated by Holman (WO 99/30240). This rejection is respectfully traversed.

Claim 1 recites: "a first data bus, said first data bus including a first bus segment and a second bus segment, each of said first bus segment and said second bus segment including a first number of data paths, and each data path of said second bus segment being separate and not directly connected to any data path of said first bus segment."

Claim 21 recites: "a first bus segment of said first data bus, said first data bus having a first number of data paths and said second data bus having a second number of data paths; a second bus segment of said first data bus, said second bus segment having said first number of data paths, each of said data paths in said second bus segment being separate and not directly connect to any of said data paths in said first bus segment."

Claims 40-41 recite: "a first data bus, said first data bus including at least a first bus segment and a second bus segment, each of said first bus segment and said second bus segment including a same plurality of data paths, and each data path of each said bus segment being separate and not directly connected to any data path of any other of said bus segments."

Claim 46 recites: "... passing data on said first data bus from said first bus segment to said second bus segment and from said second bus segment to said first bus segment via said interface circuit and wherein each of said first and second segments of

said first data bus have a same number of data paths and each data path in said first segment of said first data bus is not directly connected to any data path in said second segment of said first data bus."

Holman discloses a memory bus system in which memory modules are attached to the memory bus, and in which each memory module includes a data transfer circuit which "bridges" traffic between the memory bus and an internal memory module bus. The circuit is also capable of performing data format conversion, bus protocol conversion, and voltage conversion of signals between the two buses. However, as illustrated on, for example, Fig. 3, the system memory bus 323 of Holman is not comprised of discrete (i.e., not directly coupled) bus segments. While the Office Action is not wrong in identifying bus segments in the system memory bus 323, these segments are merely logical portions of the bus between attachment points of each memory controller 310, 316 of each memory module 306, 308. Each line 322, 324, 326, 328 of the system memory bus 323 is illustrated as a straight-through line from one end of the bus to another end.

At page 5 of the Office Action, the Examiner asserts that each component of the first data bus (i.e., lines 322, 324, 426, and 328) can be interpreted as a separate segment of the first data bus and lines 322, 324, 326, and 328 are not directly coupled to each other. In response it should be noted that line 322 corresponds a clock bus, line 324 corresponds to and command/address bus, lines 326 corresponds to a handshaking bus, and that only line 328 corresponds to a data bus. Further, claims 1, 21, 40-41, and 46 have been amended to more clearly identify the first and second bus segments.

In particular, in claims 1, 21, 40-41, 46 each of said first and second bus segments are required to have "a first number" (claims 1 and 21), "a same plurality" (claims 40-41), or "a same number" (claim 46) of data paths, and each data path in each

bus segment are not directly connected to any other data path in any other bus segment. It is respectfully submitted that these features, as recited in the above reproduced portions of claims 1, 21, 40-41, and 46 distinguish over the teachings of Holman, as Holman's data lines (328) are each shown in, for example, Fig. 4, to be a straight continuous line, i.e., a single segment having the same data paths throughout. Within each of the logical segments identified by the Office Action, all data paths are directly coupled.

Claims 43 recites "a bus system having N data paths, where N is less than M, for exchanging data between said processor and said data devices, which loops through each of said interface devices."

The Office Action asserts at page 5 that "it is clear that the system bus of Holman ... "loops through" interface device or circuits 310, 316." Reconsideration is requested. Holman at Fig. 3 clearly shows a system bus 323 comprising lines 322, 324, 326, and 328 which runs starting from a system controller 304 to the end of the bus. The data lines 328 can be said to have N data paths. The communications lines in each memory device (e.g., device 352, lines 330, 332, 334-337) can be said to have M data paths, with M being greater than N. The system bus (including each of its lines 323, 324, 326, and 328) are shown in the drawing to be directly attached to the memory module controller 310, 316. No looping structure is evident in the system memory bus 323 nor its lines 322, 324, 326, 328. In contrast, the claims require a bus system with N data paths, which loops, as shown for example, in the application by bus 28 in each of Figs. 4, 5, and 6.

Thus, claims 1, 21, 40-41, 43, and 46 are believe to be allowable over the prior art of record. Depending claims 2-20, 22-39, 44-45, and 47-61 are also believed to be

allowable over the prior art of record for at least the same reasons as their respective independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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